Notice of Allowability	Application No.	Applicant(s)	
	10/795,996	YAGI, SATOSHI	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 8/23/2006*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dan Stanger (Reg. No. 32,846) on 9/29/2006.

The following claims have been amended as follows:

7. A disk array device, comprising:

a host interface for receiving write data to be stored in a disk drive from an information processing device;

a data controller that transfers in block units the write data received by the host interface to the disk drive;

a processor for exercising overall control; and

memory for storing data,

wherein:

the processor reads serial data from the disk drive in block units and temporarily stores this serial data in the memory;

the processor compares a logical block address of a write destination of the received write data with a logical block address of the serial data read from the disk drive and temporarily stored in the memory;

when the logical block address of the write destination of the received write data is the same as the logical block address of the serial data read from the disk drive and temporarily stored in the memory, the processor updates the serial data temporarily stored in the memory by means of the received write data so that the updated serial data is available to be compared to the next-received write data; and

when the logical block address of the write destination of the received write data is different from the logical block address of the serial data read from the disk drive and temporarily stored in the memory, the processor generates a security code based on the serial data temporarily stored in the memory and according to the order of storage areas of the disk drive, adds the generated security code to the serial data temporarily stored in the memory, transfers in block units this data having the security code added thereto to the disk drive, reads the serial data stored in the block of the disk drive constituting the write destination of the received write data, and updates the serial data thus read and stored in the memory by means of the write data so that the updated serial data is available to be compared to the next-received write data.

8. A disk array device, comprising:

a channel control unit for receiving write data to be stored in a disk drive from an information processing device;

a disk control unit that performs processing relating to the writing of data to the disk drive; and

a cache memory for storing data that is exchanged between the channel control unit and the

disk control unit,

wherein:

the channel control unit comprises a data receiver for receiving the write data; a data control unit for transferring in block units the write data received by the data receiver to the cache memory; and a data storage unit for storing serial data received from a storage area of the disk drive;

the disk control unit reads serial data stored In the disk drive in block units from the cache memory and then temporarily stores this serial data in the data storage unit;

the disk control unit compares a logical block address of a write destination of the received write data with a logical block address of the serial data read from the cache memory and temporarily stored in the data storage unit;

when the logical block address of the write destination of the received write data is the same as the logical block address of the serial data read from the disk drive and temporarily stored in the data storage unit, the data control unit updates the serial data temporarily stored in the data storage unit by means of the received write data so that the updated serial data is available to be compared to the next-received write data; and

when the logical block address of the write destination of the received write data is different from the logical block address of the serial data read from the disk drive and temporarily stored in the data storage unit, the data control unit generates a security code based on the serial data temporarily stored in the data storage unit and according to the order of storage areas of the disk drive, adds the generated security code to the serial data temporarily stored in the data storage unit, transfers in block units this serial data having the security code added

thereto to the cache memory, reads the serial data stored in the block of the disk drive constituting the write destination of the received write data from the cache memory, and updates the data thus read and stored in the data storage unit by means of the write data so that the updated serial data is available to be compared to the next-received write data.

10. A disk array device, comprising:

a channel control unit for receiving write data to be stored in a disk drive from an information processing device;

a disk control unit that performs processing relating to the writing of data to the disk drive; and

a cache memory for storing data that is exchanged between the channel control unit and the disk control unit,

wherein:

the disk control unit comprises a data read unit, which reads the write data from the cache memory, a data control unit which transfers in block units the write data read by the data read unit to the disk drive; and a data storage unit for storing serial data received from a storage area of the disk drive;

the disk control unit reads the serial data from the disk drive in block units and then temporarily stores this serial data in the data storage unit;

the disk control unit compares a logical block address of a write destination of the received write data with a logical block address of the serial data read from the disk drive and temporarily stored in the data storage unit;

when the logical block address of the write destination of the received write data is the same as the logical block address of the serial data read from the disk drive and temporarily stored in the data storage unit, the data control unit updates the serial data temporarily stored in the data storage unit by means of the write data read from the cache memory so that the updated serial data is available to be compared to the next-received write data; and

when the logical block address of the write destination of the received write data is different from the logical block address of the serial data read from disk drive and temporarily stored in the data storage unit, the data control unit generates a security code based on the serial data temporarily stored in the data storage unit and according to the order of the storage areas of the disk drive, adds the generated security code to the serial data temporarily stored in the data storage unit before transferring in block units this serial data having the security code added thereto to the disk drive, reads the serial data stored in the block of the disk drive constituting the write destination of the received write data, and updates the data thus read and stored in the data storage unit by means of the write data so that the updated serial data is available to be compared to the next-received write data.

Reasons for Allowance

Prosecution for this application has been assumed by Examiner Shane Thomas. Pursuant to MPEP §704.01, the previous Examiner's search has been given full faith and credit, and as such, only a cursory search of the prior art has been made by the present Examiner. The amendment filed 8/23/2006, in addition to the Examiner's amendment above place the claims in condition for allowance. The Applicant's arguments regarding the amended claims (pages 16-18 of the 8/23/2006 response) have been considered by the present Examiner and are persuasive; thus, the present claims overcome the prior art of record.

Claims 1-12 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance:

As per claims 1,3,5,7,8,10, and 11, as argued by the Applicant, the prior art of record does not specifically teach, or suggest either alone or in combination, (1) the generation of a security code within a "data storage unit" (e.g. disk cache) based on the data stored therein *and* an order of storage areas of the disk drive, and (2) transferring the serial data having the security code added thereto to the disk drive in block units, when both limitations are taken in the context of the claim as a whole.

Bearden (U.S. Patent Application Publication No. 2004/0205299) teaches a method for disk cache hit/miss and appending ECC data (security data) to a block of data before being written to the disk drive (¶33), but does not specifically teach the aforementioned limitations of generating the ECC data based on the order of storage areas of the disk drive as well as transferring serial data from the disk cache to the disk drive in [whole] block units.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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